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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,781	07/22/2003	Qiuyi Ye	BUR900090US2	6787

30400 7590 10/18/2004

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EXAMINER	
LINDSAY JR, WALTER LEE	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 10/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/624,781	YE ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *6-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/22/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Election filed on 8/26/2004.

Currently claims 1-14 are pending. Claims 1-5 are withdrawn.

Election/Restrictions

1. Claims 1-5 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected device, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 8/26/2004.

2. Applicant's election with traverse of claims 6-14 in the reply filed on 8/26/2004 is acknowledged. The traversal is on the ground(s) that the inventions would have a similar field of search. This is not found persuasive because, the search for the semiconductor structure is contained in class 257 and consists of finding a FET, with a cap free gate, having insulating sidewall spacer on said gate having a height less than or equal to a height of the cap-free gate, wherein the search for the method is contained in class 438 and consists of no height parameters that the spacer is forced to meet.

The requirement is still deemed proper and is therefore made FINAL.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the terms "film", "hole", and "opening", as found in claims 6-14, are not clearly distinguished in the written description of the Best Mode for Carrying

Out Invention section of the Specification. For examination purposes only, at this time, the Examiner defines these terms as follows:

"film"- polysilicon film (108) (fig. 2 of Applicant's drawings);

"hole"- the region defined by the top of the polysilicon film (108) to the substrate(102), and resulting from the gate patterning step (fig. 2 of Applicant's drawings);

"opening"- the region defined above the top of polysilicon film (108) to the top of the dielectric layer (122) and above (fig. 5 of Applicant's drawings).

4. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 10, 11 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claims 10, 11 and 13 recite the limitation "said conductive material" in line 1 of each claim respectively. There is insufficient antecedent basis for this limitation in the claims. Claim 6 contains no mention of a "conductive material". It is suggested that claims 10, 11 and 13 should depend from claim 9.

For examining purposes only, the limitation "said conductive material" will be treated as " said material" in claims 10, 11, and 13 since they depend from claim 6 at this time.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 6-10, and 12-14 rejected under 35 U.S.C. 102(e) as being anticipated by Kinoshita et al. (U.S. Patent No. 6,271,087 filed on 10/10/2000).

Kinoshita shows the method as claimed, in Fig. 3A-3E (transistor, 210 c) and corresponding text as: providing a substrate (102) (fig. 3A) (col. 6, lines 38-43); forming a film on said substrate (gate film, (224)), said film having a top surface (top of (224)) (Fig. 3c) (col. 7, lines 21-25); forming a hole (gate patterning step. Hole extends from top of gate through film (224) to the substrate) through said film (Fig. 3A) (col. 6, lines 38-43); providing an insulating layer (232) having an opening (235) aligned to the hole and larger than the hole so a portion of said top surface of said film is exposed (Fig. 3C) (col. 7, lines 21-25); providing a material ((239), portion from substrate to top of the (224)) in said hole (Fig. 3D) (col. 7, lines 26-40); providing a spacer ((239), portion from top of (224) to the top of and above (232)) along a sidewall of said opening to shrink said opening and cover exposed portions of said top surface of said film, wherein said spacer extends to said material within the hole(Fig. 3E) (col. 7, lines 41-45) (claim 6). [To further clarify the examiner's position regarding the material provided in the "hole"

and the spacer provided in the opening. The material deposited into the "hole" correlates to the region of material (239) that is formed between the substrate and the top of layer (224), and the spacer is the region of material (239) from the top of (224) to the top of (232) and above. This allows steps E and F, the ability to be performed simultaneously.] Kinoshita teaches that the film (224) is conductive, and said film is borderless to said material (239) in said hole (Fig. 3D) (col. 7, lines 26-40) (claim 7). Kinoshita teaches the step of providing an insulating spacer (230) along a sidewall of said hole to insulate said sidewall of said conductive film, thereby allowing said borderless contact (Fig. 3E) (col. 7, lines 41-45) (claim 8). Kinoshita teaches that the material in said hole is conductive (Fig. 3D) (col. 7, lines 26-40) (claim 9). Kinoshita teaches that the material comprises a metal or conductive polysilicon (Fig. 3D) (col. 7, lines 30-35) (claim 10). Kinoshita teaches that the film comprises a substantially cap-free gate conductor of a field effect transistor (210c) (Fig. 3E) (col. 7, lines 41-45) (claim 12). Kinoshita teaches that the material is a conductive contact to a diffusion (202c) (Fig. 3E) (col. 7, lines 41-45) (claim 13). Kinoshita teaches that providing an insulating layer comprises forming an opening in a hard mask (Fig. 3C) (col. 7, lines 5-10) (claim 14).

10. Claims 6 and 9-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Nesbit et al. (U.S. Patent No. 6,686,668 filed 1/17/2001).

Nesbit shows the method as claimed, in Fig. 5-9 and corresponding text as: providing a substrate (5) (Fig. 2) (col. 4, lines 32-46); forming a film on said substrate (20, gate film), said film having a top surface (top of 20) (Fig. 2) (col. 4, lines 32-46);

forming a hole through said film (gate patterning step. Hole extends through top of gate film 20 to the substrate) (Fig. 2) (col. 4, lines 32-46); providing an insulating layer (35 and 40) having an opening aligned to the hole and larger than the hole so a portion of said top surface of said film is exposed (Fig. 6) (col. 5, lines 1-6); providing a material (45) in said hole (Figs. 7-8) (col. 5, lines 7-13); providing a spacer (50, film overlying the material in hole) along a sidewall of said opening to shrink said opening and cover exposed portions of said top surface of said film, wherein said spacer extends to said material within the hole(Fig. 9) (col. 5, lines 14-22) (claim 6). Nesbit teaches that the material in said hole is conductive (Figs. 7-8) (col. 5, lines 7-13) (claim 9). Nesbit teaches that the material comprises a metal or conductive polysilicon (Figs. 7-8) (col. 5, lines 7-13). Nesbit teaches that the material is recessed below said top surface of said film (Fig. 8) (col. 5, lines 12-13) (claim 11).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John F Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
September 29, 2004